

MECHANISM FOR IMPLEMENTING CACHE LINE FILLS

Abstract of the Disclosure

The present invention provides a mechanism for implementing cache line fills. In response to a target address, a decoder generates primary and secondary look-ups to a first cache on standard and pseudo ports, respectively. Responsive to miss by the primary access, a data block is returned to the first cache, the data block having a size determined by a hit/miss signal generated by the secondary look-up.

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